Abstract

A gate structure is disclosed with improved endurance characteristics. Source and drain regions are contained within a semiconductor region of a substrate. At least a gate stack, which is disposed over the semiconductor region, is situated between the source and drain regions. The gate stack contains a gate insulator layer formed over the semiconductor region, a conductive gate layer disposed over the gate insulator layer, a top gate stack layer disposed over the conductive gate layer. A sidewall insulator layer is disposed over sidewalls of the gate stack. Nitrogen atoms are incorporated along the conductive gate layer sidewall-sidewall insulator layer interface and along the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge.